

Time: 3 Hours

Marks: 80

Instructions:

1. Assume suitable **data** if necessary.
2. Question **No.1** is **Compulsory**.
3. Solve any **Three** Questions from **Q.2 to Q.6**.
4. Figures to Right Indicates **Marks**.

Q1) Solve **any Four**.

(20 Marks)

- a. Explain voltage transfer characteristics (VTC) of CMOS inverter.
- b. Implement a 2x1 multiplexer using CMOS transmission gates (TG).
- c. Explain 1T DRAM cell.
- d. Draw 4x4 NAND- based ROM array (using Transistor) memory for following table,

R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	1	1	0	1
0	1	0	0	1	0	0	1
0	0	1	0	1	0	1	0
0	0	0	1	1	0	0	1

- e. Explain short channel effects in VLSI.
- f. Define Channel Pinch-off with condition and Write drain current equations for Linear and Saturation region.

Q2) Solve the following.

(20 Marks)

- a. Compare the two technology scaling methods, namely, (i) the constant electric-field scaling and (ii) the constant power-supply voltage scaling. In particular, show analytically by using equations how the **oxide capacitance, drain current in saturation, and power dissipation** are affected in terms of the scaling factor, S.
- b. Consider a CMOS inverter circuit with $V_{DD} = 3.3 \text{ V}$, $k_n = 200 \mu\text{A/V}^2$, $k_p = 80 \mu\text{A/V}^2$, $V_{thn} = 0.6 \text{ V}$, $V_{thp} = -0.7 \text{ V}$, $k_r = 2.5$. Calculate the critical voltages (V_{OL} , V_{OH} , V_{IL} , V_{IH}) on the VTC and find the noise margins of the circuit.

Q3) Solve the following.

(20 Marks)

- a. Draw and explain 6T-SRAM Memory.
- b. Explain steps for fabrication process of a CMOS transistor with neat diagram.

Q4) Solve the following.

(20 Marks)

- a. Draw an RTL of 4-bit Ripple Carry Adder (RCA) and Carry Save Adder (CSA).
- b. Implement a following function using Static CMOS, Pseudo NMOS, Dynamic CMOS and Domino Logic.

$$Y = A.B$$

5) Solve the following.

(20 Marks)

- a. Draw a CMOS Logic and Physical layout for 2-input NAND Gate.
- b. Draw and explain 3T-DRAM memory.

Q6) Solve the following.

(20 Marks)

- a. Implement using CMOS Logic 1-bit Full adder and D latch using Transmission Gates (TG).
- b. Write a short note on Clock Generation, Distribution and ESD Protection.
